8088/86 Processor Timing
Write Cycle

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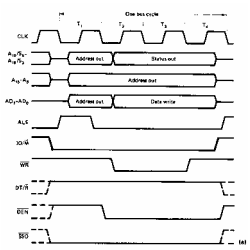
Write Memory Cycle

Section 8.11

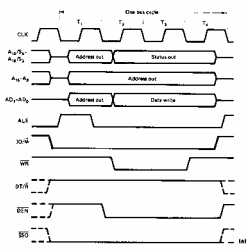


T1

- Output 20 bit address on A0-A19
- ALE goes active at same time
- Latching of the multiplexed address (AD0-AD7) occurs on Falling edge of ALE
- IO/M set to 0 indicating memory operation is in progress
- DT/R is set to 1, (transmission)

Write Memory Cycle

(cont)



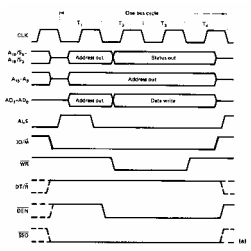
T2

- A16-A19 output Status bits S3-S6
- AD0-AD7 put in HIGH Z
- A8-A15 are maintained

- T2+
  - WR is set low (indicating a write operation)
  - DEN is set low (enable external circuitry to allow data to move to memory from the processor)

Write Memory Cycle

(cont)

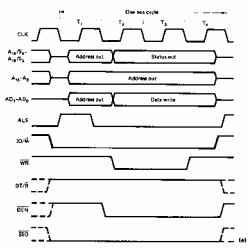


T3

- Data Write

Write Memory Cycle

(cont)

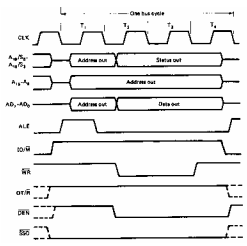


T4

- WR goes high
- DEN goes to inactive state
- Write cycle ends

Write - Output Cycle

Section 8.18 (partial)



Writing to an Output Port is similar to the Write Memory cycle except the IO/M line does not go low in T1 (indicating it is a IO function, not memory)

Address Latch

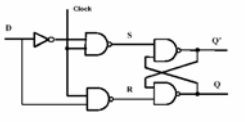
AD0-AD7 are multiplexed

- T1 – they are address lines
- T3 – they are data lines

How can we have the FULL Physical address available when we read/write to memory or I/O?

D-Latch

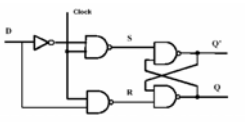
- When Clock is inactive (low) the outputs (Q and Q') are kept at their previous values
- When Clock is Active, the input (D) is copied to the output.



Clk	D	Q(t+1)
0	0	Q(t)
0	1	Q(t)
1	0	0
1	1	1

D-Latch

- We know that in T1
  - AD0-AD7 contains the low byte of the address
  - ALE is LOW



So we can use Ð LATCHES to hold the address data when ALE goes LOW

Clk	D	Q(t+1)
0	0	Q(t)
0	1	Q(t)
1	0	0
1	1	1

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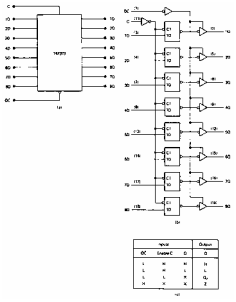

So Now……

From this weeks lab: